Claims:

Claims 18-20 (cancelled);

Claim 21.(new) A printed-circuit-board-under-test (PCB-UT), comprising:

a first integrated circuit chip having a substrate circuit and at least one non-electrically-programmable three-dimensional memory (NEP-3DM) level, said substrate circuit comprising a circuit-under-test (CUT), and said NEP-3DM level being stacked on said substrate circuit;

a second integrated circuit chip;

wherein said NEP-3DM level stores at least a portion of test data and/or test-data seeds for said first and second integrated circuit chips.

Claim 22. (new) The PCB-UT according to claim 21, further comprising a test interface, whereby said NEP-3DM level can be tested through said test interface.